This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Original): A switched-capacitor power supply comprising:

(a) a plurality of thin-film capacitors each one of said plurality of thin-film capacitors being disposed substantially along a first plane and elongated to have a first end and a second end;

(b) a power management integrated circuit for controlling the switched-capacitor power supply;

(c) a plurality of semiconductor switches, each selected one of which plurality of semiconductor switches being connected to one or more selected ones of the plurality of thin-film capacitors;

(d) a plurality of connective structures, each selected one of which plurality of connective structures being disposed to connect each selected one of the plurality of semiconductor switches to the one or more selected ones of the plurality of thin-film capacitors while being disposed substantially along one of a plurality of respective axes that are disposed in an orientation that is substantially normal to the first plane.

Claim 2 (Original): The switched-capacitor power supply of claim 1 in which the plurality of semiconductor switches is comprised of a charge group of semiconductor switches that when switched cause charge to flow into selected ones of the plurality of thin-film capacitors and a discharge group of semiconductor switches that when switched cause charge to flow out of selected ones of the plurality of thin-film capacitors.

Claim 3 (Original): The switched-capacitor power supply of claim 1 in which the plurality of thin-film capacitors are arranged about a grouping point so that the first end of each one of the plurality of thin-film capacitors is closer to the grouping point than is the second end.

Claim 4 (Original): The switched-capacitor power supply of claim 2 in which the plurality of thin-film capacitors are arranged about a grouping point so that the first end of each one of the plurality of thin-film capacitors is closer to the grouping point than is the second end.

Claim 5 (Original): The switched-capacitor power supply of claim 3 in which the plurality of thin-film capacitors are arranged in an arcuate disposition about the grouping point.

Claim 6 (Original): The switched-capacitor power supply of claim 4 in which the plurality of thin-film capacitors are arranged in an arcuate disposition about the grouping point.

Claim 7 (Original): The switched-capacitor power supply of claim 6 in which the arcuate disposition is a circular disposition.

Claim 8 (Original): The switched-capacitor power supply of claim 1 in which each one of the plurality of connective structures comprises a via.

Claim 9 (Original): The switched-capacitor power supply of claim 2 in which each one of the plurality of connective structures comprises a via.

Claim 10 (Original): The switched-capacitor power supply of claim 8 in which the via is a stacked via.

Claim 11 (Original): The switched-capacitor power supply of claim 9 in which the via is a stacked via.

Claim 12 (Original): The switched-capacitor power supply of claim 1 in which each one of the plurality of connective structures comprises a stacked via and a ball contact.

Claim 13 (Original): The switched-capacitor power supply of claim 2 in which each one of the plurality of connective structures comprises a stacked via and a ball contact.

Claim 14 (Original): The switched-capacitor power supply of claim 1 in which the plurality of connective structures are integrated with the power management integrated circuit.

Claim 15 (Original): The switched-capacitor power supply of claim 6 in which the plurality of connective structures are integrated with the power management integrated circuit.

Claim 16 (Original): The switched-capacitor power supply of claim 3 in which the power management integrated circuit is devised in a flip-chip construction and the plurality of thin-film capacitors and the power management integrated circuit are disposed relative to each other to establish a direct connection between the plurality of thin-film capacitors and respective ones of the plurality of connective structures integrated with the power management integrated circuit.

Claim 17 (Original): The switched-capacitor power supply of claim 4 in which the power management integrated circuit is devised in a flip-chip construction and the plurality of thin-film capacitors and the power management integrated circuit are disposed relative to each other to establish a direct connection between the plurality of thin-film capacitors and respective ones of the plurality of connective structures integrated with the power management integrated circuit.

Claim 18 (Original): The switched-capacitor power supply of claim 3 in which each one of the plurality of thin-film capacitors has a first and a second access point at its respective first end and the power management integrated circuit is devised in a BGA package that is surface

mounted to contact the first and second access points of each of the plurality of thin-film capacitors.

Claim 19 (Original): The switched-capacitor power supply of claim 4 in which each one of the plurality of thin-film capacitors has a first and a second access point at its respective first end and the power management integrated circuit is devised in a BGA package that is surface mounted to contact the first and second access points of each of the plurality of thin-film capacitors.

Claim 20 (Original): A switched-capacitor power supply comprising:

(a) a plurality of capacitors formed on a substrate, the capacitors having a plurality of electrodes;

(b) a plurality of charging transistors formed on an integrated circuit;

(c) a plurality of discharging transistors formed on the integrated circuit;

(d) a plurality of conducting structures connecting a plurality of respective terminals of the charging and discharging transistors to respective ones of the capacitor electrodes, the conducting structures having an equivalent series resistance of less than 10 milliohms.

Claim 21 (Original): The switched-capacitor power supply of Claim 20 wherein the conducting structures have a partial inductance of less than 50 pico-henries.

Claim 22 (Original): The switched-capacitor power supply of Claim 20 wherein the conducting structures comprise bumps.

Claim 23 (Original): The switched-capacitor power supply of Claim 20 wherein the conducting structures comprise vias.

Claim 24 (Original): The switched-capacitor power supply of Claim 20 wherein the conducting structures comprise stacked vias.

Claim 25 (Original): The switched-capacitor power supply of Claim 20 wherein the capacitors are thin-film capacitors.

Claim 26 (Original): The switched-capacitor power supply of Claim 20 wherein the capacitors have a equivalent series inductance of less than 1 pico-henry.

Claim 27 (Original): The switched-capacitor power supply of Claim 20 wherein the capacitors have a equivalent series resistance of less than 100 milliohms.

Claim 28 (Original): The switched-capacitor power supply of Claim 20 wherein a plurality of the capacitors are elongated and have a proximal end, the proximal ends being grouped near the integrated circuit.

Claim 29 (Original): The switched-capacitor power supply of Claim 20 wherein the charging and discharging transistors have a gate capacitance of less than 2 pico-farads.

Claim 30 (Original): The switched-capacitor power supply of Claim 20 wherein the charging and discharging transistors are N-channel FETs.

Claim 31 (Original): A method of charging and discharging a plurality of capacitors in a switched-capacitor power supply, the method comprising:

(a) applying a charging current to the capacitors through a plurality of charging transistors on an integrated chip, the charging transistors arranged in a layout such that a plurality of respective terminals of the respective charging transistors are disposed above a portion of a plurality of respective electrodes of the plurality of capacitors;

(b) applying an output current from the capacitors through a plurality of discharging transistors on the integrated chip, the discharging transistors arranged in a layout such that a plurality of respective terminals of the respective discharging transistors are disposed above a portion of a plurality of respective electrodes of the plurality of capacitors.

Claim 32 (Original): A power supply system comprising:

(a) at least one phase comprising:

(i) a plurality of thin-film capacitors arranged with an at least one P1 transistor electrically between respective adjacent pairs of the plurality of thin-film capacitors connecting the plurality of capacitors in series, the plurality of capacitors each having a positive terminal and a negative terminal;

(ii) at least one P2 transistor connecting the positive terminal of at least one of the plurality of capacitors to a voltage input terminal;

(iii) at least one P5 transistor connecting the positive terminal of at least one of the plurality of thin-film capacitors to an output terminal; and

(iv) a plurality of P4 transistors connecting the respective negative terminals of the plurality of capacitors to a reference potential.

(b) a controller operatively connected to all of the transistors, the controller operative to switch the transistors between a first charging mode in which all of the P4 and P5 transistors in the phase are de-activated, and a second discharging mode in which all of the P1 and P2 transistors in the phases are de-activated.

Claim 33 (Original): The power supply system of Claim 32 wherein the thin-film capacitors comprise elongated structures arranged having a longitudinal axis oriented to point substantially toward the controller.

Claim 34 (Original): The power supply system of Claim 32 wherein the P1, P2, P4, and P5 transistors are disposed in a layout on a power management IC, the layout substantially matching a layout of a plurality of connecting electrodes of respective thin-film capacitors in a manner devised to place respective terminals of the P1, P2, P4, and P5 transistors substantially along a plurality of axes perpendicular to the longitudinal axes of the thin-film capacitors.

Claim 35 (Original): The power supply system of Claim 32 wherein a layout of the P4 and P5 transistors on a power management IC substantially matches a layout of a plurality of connecting points to their respective thin-film capacitors.

Claim 36 (Original): The power supply system of Claim 32 wherein a layout of the P1 and P2 transistors on a power management IC substantially matches a layout of a plurality of connecting points to their respective thin-film capacitors.

Claim 37 (Original): The power supply system of Claim 32 further comprising a delay-locked loop having an input connected to an oscillator and a plurality of delay stages presenting a plurality of phase-delayed oscillator signals operatively connected to respective ones of the plurality of switched-capacitor phases.

Claim 38 (Original): The power supply system of Claim 32 further including a plurality of P3 transistors connected in parallel with the plurality of P4 transistors and operatively connected to the controller, the controller operable to activate P3 transistors slightly in advance

of the P4 transistors, the P3 transistors having an ON resistance substantially higher than an ON resistance of the P4 transistors.

Claim 39 (Original): The power supply system of Claim 32 wherein the P1, P2, P4, and P5 transistors have a gate capacitance of less than 2 pico-farads.

Claim 40 (Original): The power supply system of Claim 32 wherein the P1, P2, P4, and P5 transistors are N-channel FETs.

Claim 41 (Original): The power supply system of Claim 32 wherein the P1, P2, P4, and P5 transistors are FETs having a channel length of about 0.18 micro-meters or less.

Claim 42 (Original): A method of controlling a switched-capacitor power supply comprising the steps:

(a) allocating a plurality of thin-film switched-capacitor phases to supply at least one load;

(b) sensing a difference between a desired load voltage and an actual load voltage;

(c) in response to a higher desired voltage at a substantially constant load current, allocating at least one additional switched-capacitor phase to the load or removing an at least one capacitor block from at least one of the switched-capacitor phases;

(d) in response to a lower desired voltage at a substantially constant load current, de-allocating at least one of the switched-capacitor phases or adding at least one capacitor block to an at least one switched capacitor phase.

Claim 43 (Original): The method of Claim 42 further including the steps:

(a) receiving a required-voltage instruction from the at least one load;

(b) in response to a difference in the required-voltage instruction and a past-required voltage, allocating or de-allocating an at least one switched-capacitor phase to the load or an at least one capacitor block from at least one of the switched-capacitor phases.

Claim 44 (Original): The method of Claim 42 further including the steps:

(a) receiving a required-current instruction from the at least one load;

(b) in response to a difference in the required-current instruction and a past-required current value, allocating or de-allocating an at least one switched-capacitor phase to the load or an at least one capacitor block from at least one of the switched-capacitor phases.

Claim 45 (Original): A method of operating a switched-capacitor power supply having a plurality of switched-capacitor phases each having a plurality of capacitors, the method comprising the steps:

(a) de-activating a plurality of P1 transistors connected to a positive terminal of at least one of the capacitors;

(b) de-activating at least one P2 transistor connecting at least one of the capacitors in each phase of the capacitors to an input supply voltage;

(c) after de-activating the P1 and P2 transistors in each phase, activating a P3 transistor connecting a negative terminal of each of the capacitors to ground; and

(d) after activating the P3 transistors, activating a P4 transistor connecting a negative terminal of each of the capacitors to ground and activating a P5 transistor connecting the positive terminal of at least one of the capacitors to an output terminal.

Claim 46 (Original): The method of Claim 45 in which the steps are performed for each phase in an interleaved timing arrangement.

Claim 47 (Original): The method of Claim 45 further including the steps of:

(a) activating the plurality of P1 transistors; and then

(b) waiting until a voltage across the at least one P2 transistor is substantially lowered; and then

(c) activating the at least one P2 transistor.

Claim 48 (Currently Amended): A voltage converter system comprising:

(a) a plurality of capacitors, each having a positive terminal and a negative terminal, arranged in one or more phases with one or more charging switches electrically between respective pairs of the capacitors in each phase;

(b) one or more voltage supply switches connecting the positive terminal of a respective one or more of the plurality of capacitors to a voltage input terminal;

(c) one or more first discharging switches connecting the positive terminal of a respective one or more of the plurality of capacitors to an output terminal for that phase;

(d) one or more second discharging switches connecting the negative terminals of respective ones of the plurality of capacitors to a selected reference potential;

(e) one or more voltage-shifting switches, connected in parallel with the one or more second discharging switches ~~switches~~;

(f) a control stage operatively connected to all of the switches, the control stage operative to activate and de-activate selected ones of the switches of a selected phase to change between a first charging mode and a second discharging mode, the control stage operative to activate selected ones of the voltage-shifting switches of the selected phase prior to activating selected ones of the second discharging switches ~~switches~~.

Claim 49 (Original): The voltage converter system of Claim 48 in which the control stage is operative to activate the one or more charging switches of the selected phase prior to activating the one or more voltage supply switches of the selected phase.

Claim 50 (Original): The voltage converter system of Claim 48 in which the number of phases is more than one and the control stage is operative to activate the first charging and second discharging modes for selected phases in an interleaved order.

Claim 51 (Original): The voltage converter system of Claim 50 in which the control stage is operative to deactivate selected switches at the end the second charging mode after a charging current becomes substantially lower than an initial charging current.

Claim 52 (Original): The voltage converter system of Claim 50 in the capacitors are thin-film capacitors.

Claim 53 (Original): The voltage converter system of Claim 52 in which the capacitors are formed on a common substrate.

Claim 54 (Original): The voltage converter system of Claim 50 in which the number of phases is 4 or more and the controller is operative to allocate and operate two or more phases to supply at each of two or more power loads.

Claim 55 (Original): The voltage converter system of Claim 54 in which at least two of the two or more power loads are power domains on a single IC.